Phase 2 Report

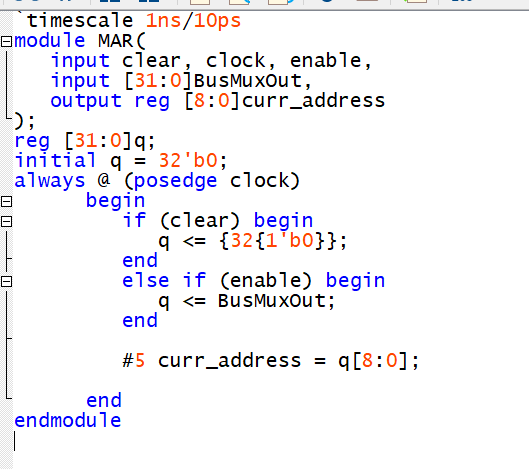
Matteo Van Der Platt, Jacob Badali, Sean Lawrence

*“We do hereby verify that this written lab report is our own work and contains our own original ideas, concepts, and designs. No portion of this report has been copied in whole or in part from another source, with the possible exception of properly referenced material"*

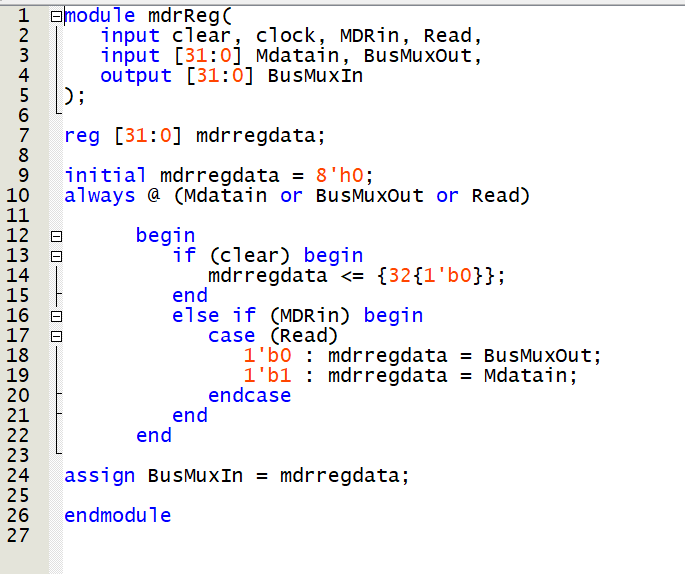
# Verilog Code

## Memory Subsystem

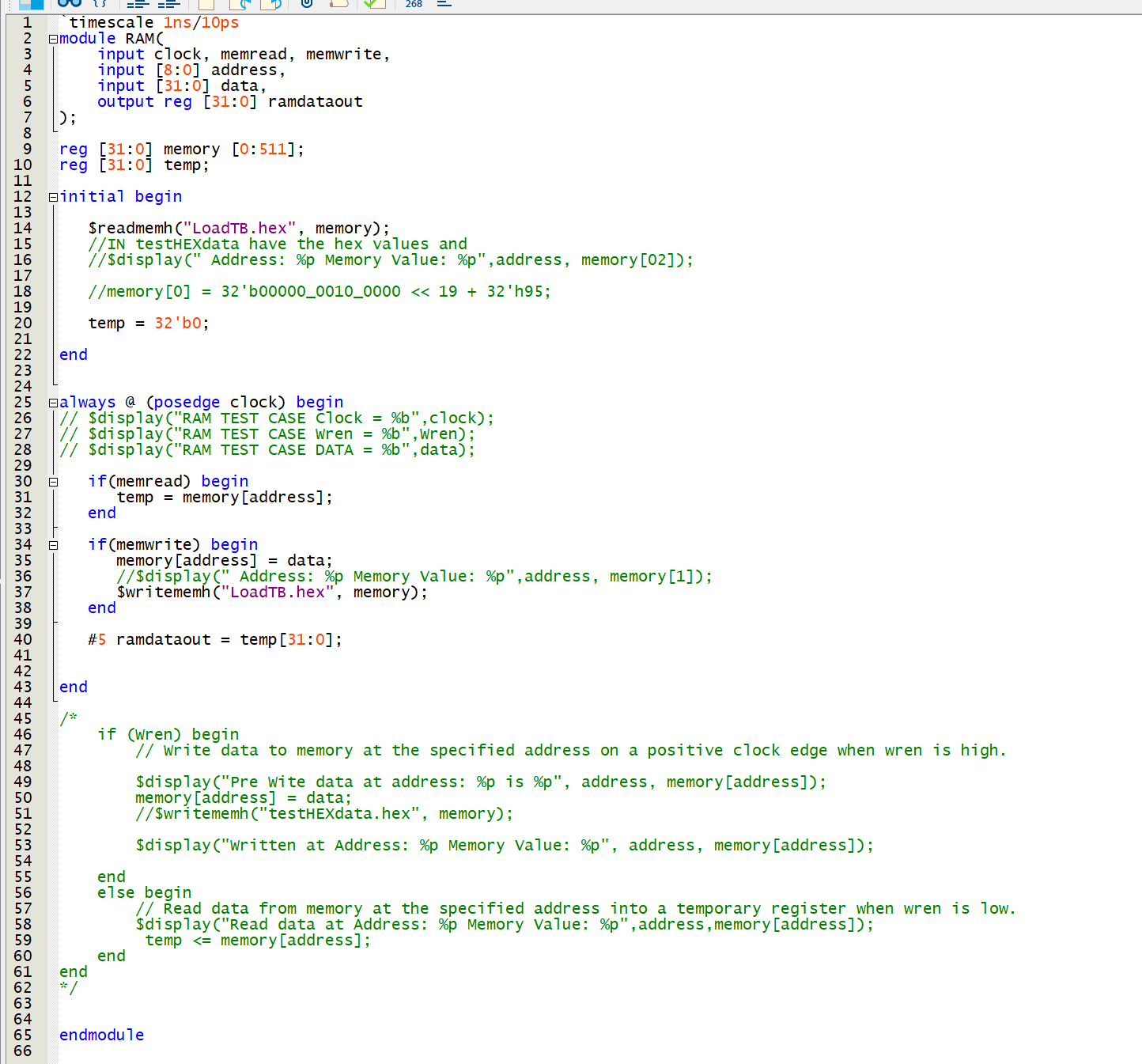
### MAR



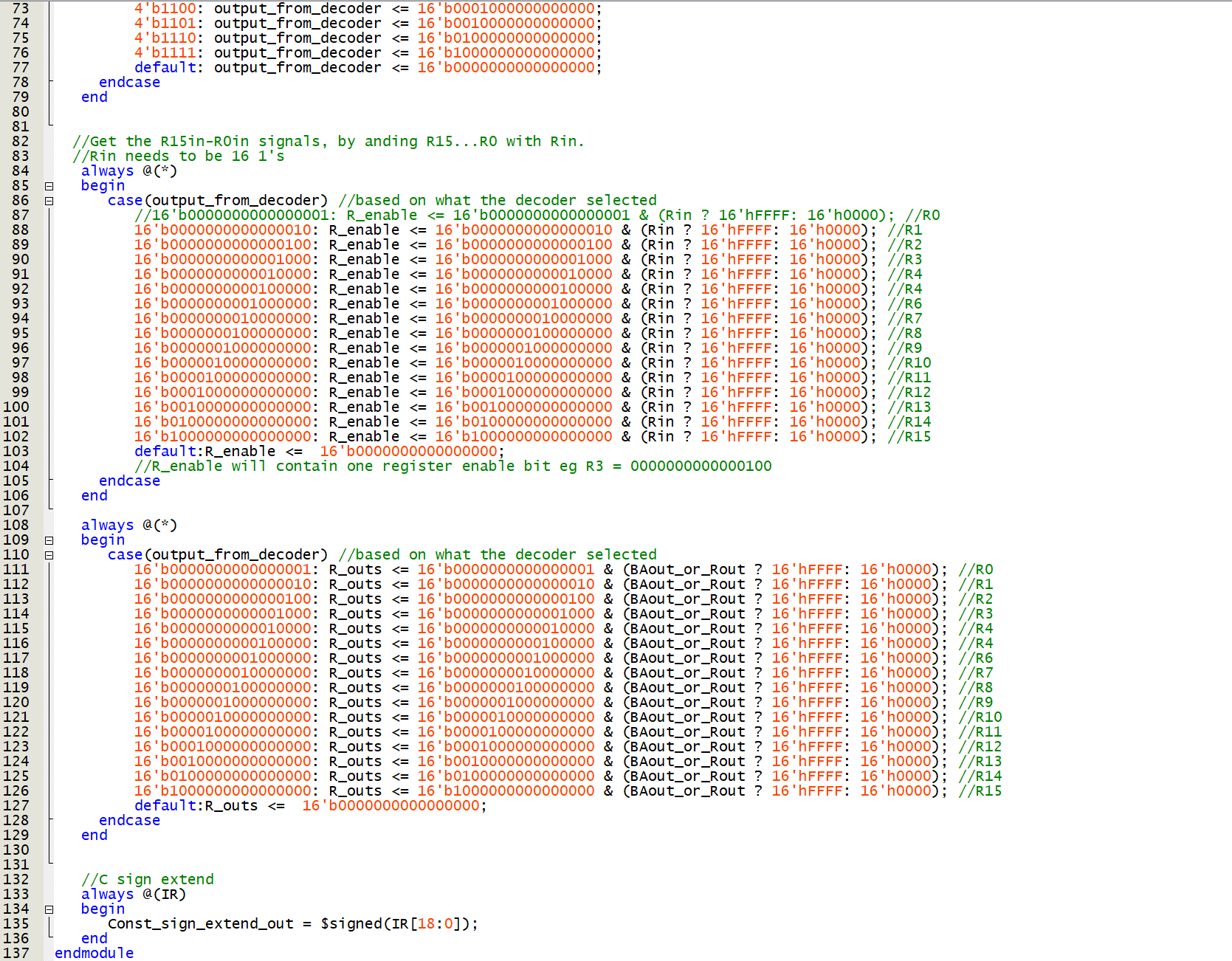
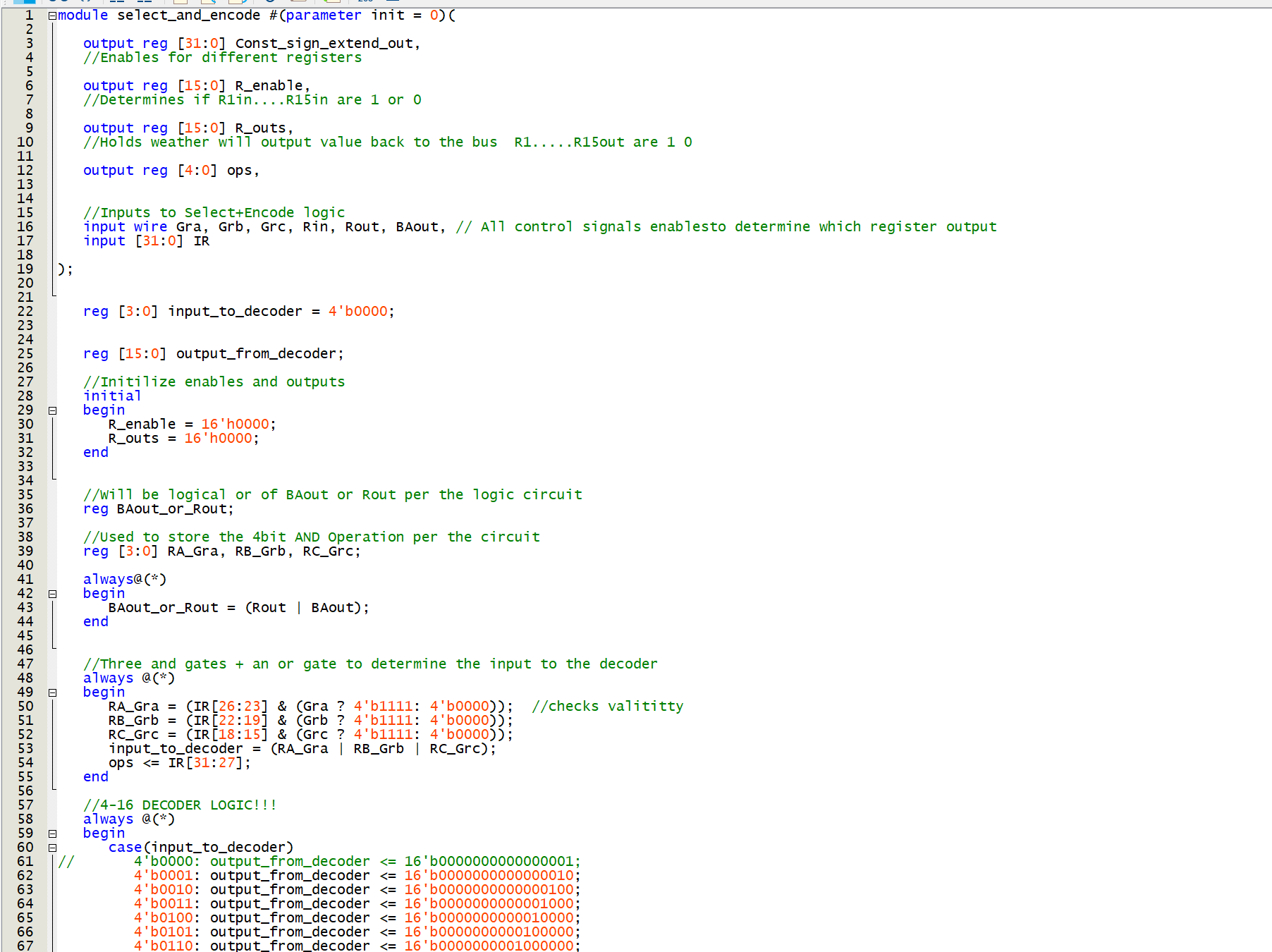
### MDR



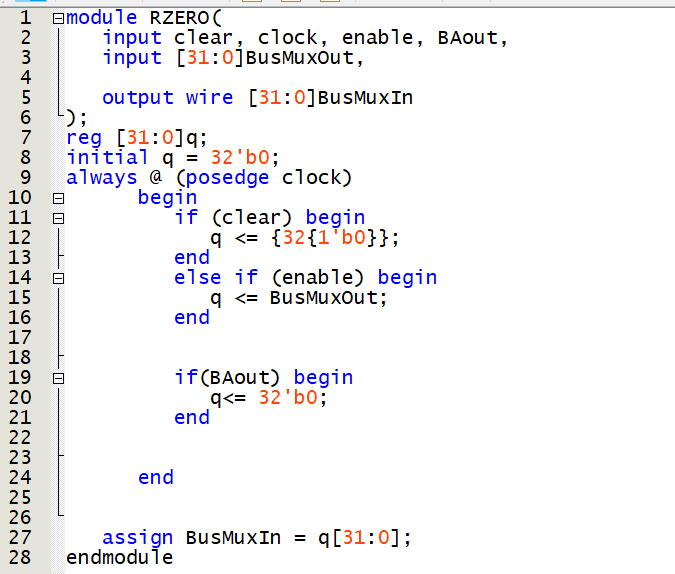
### RAM



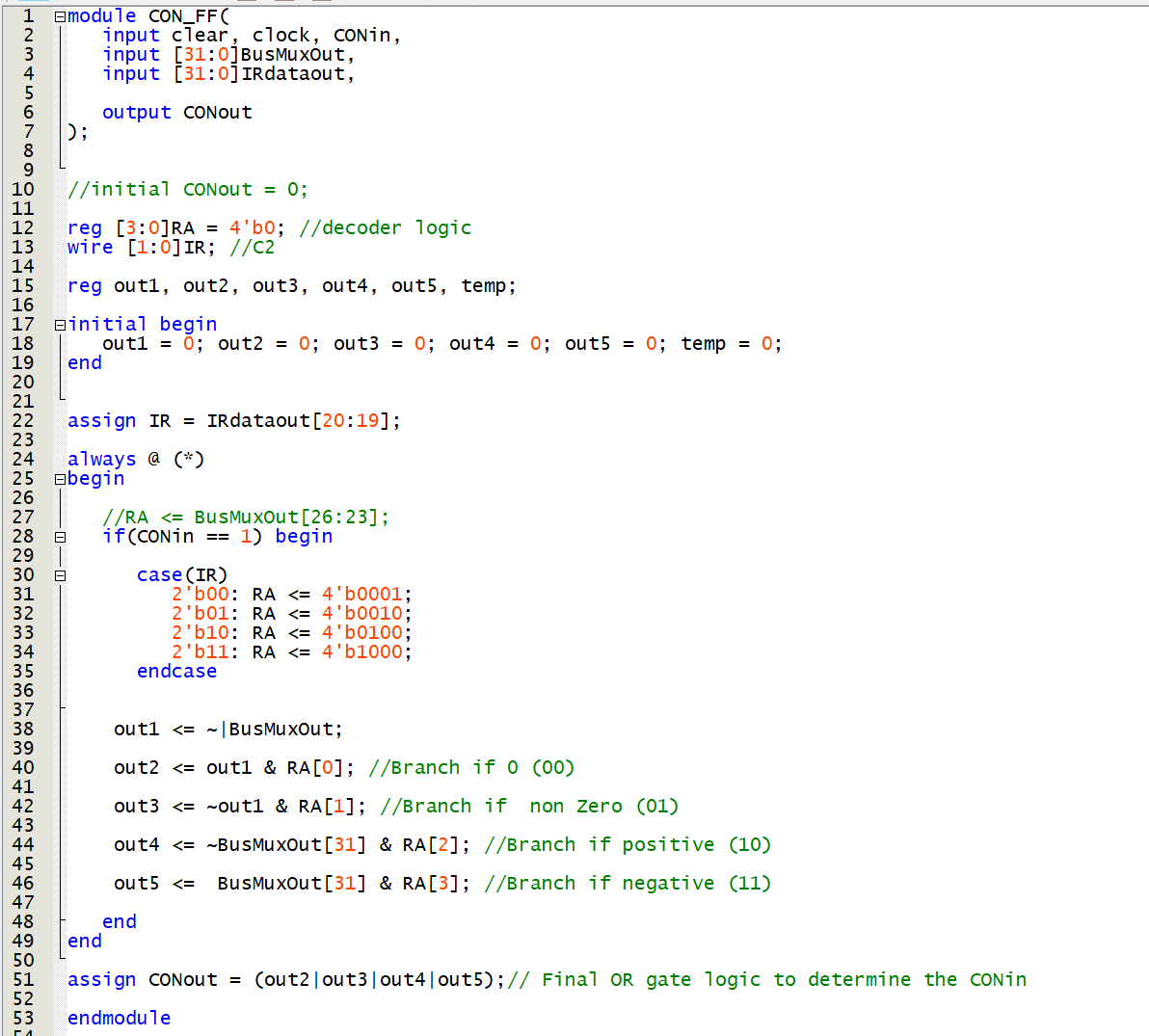
## Select and Encode Logic



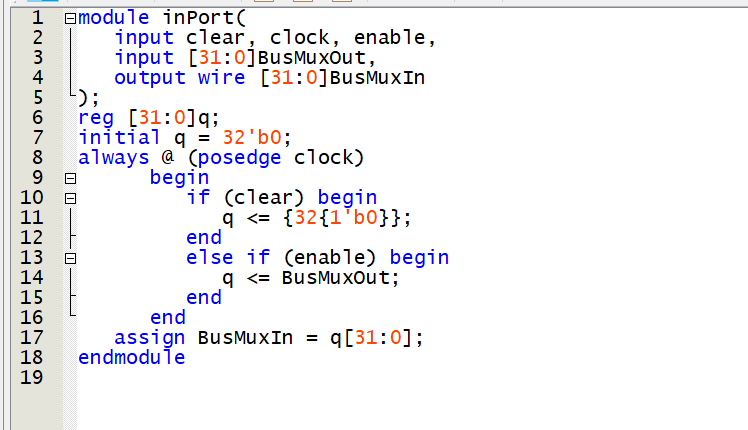
## Revision to R0

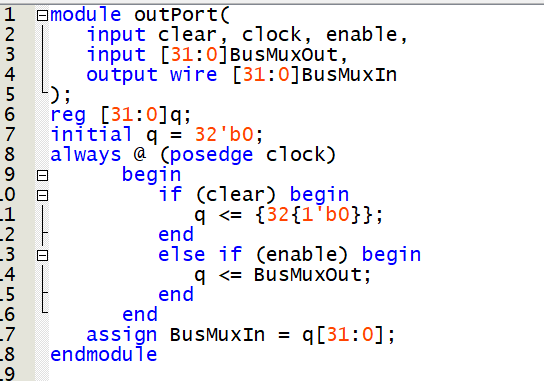


## CONFF



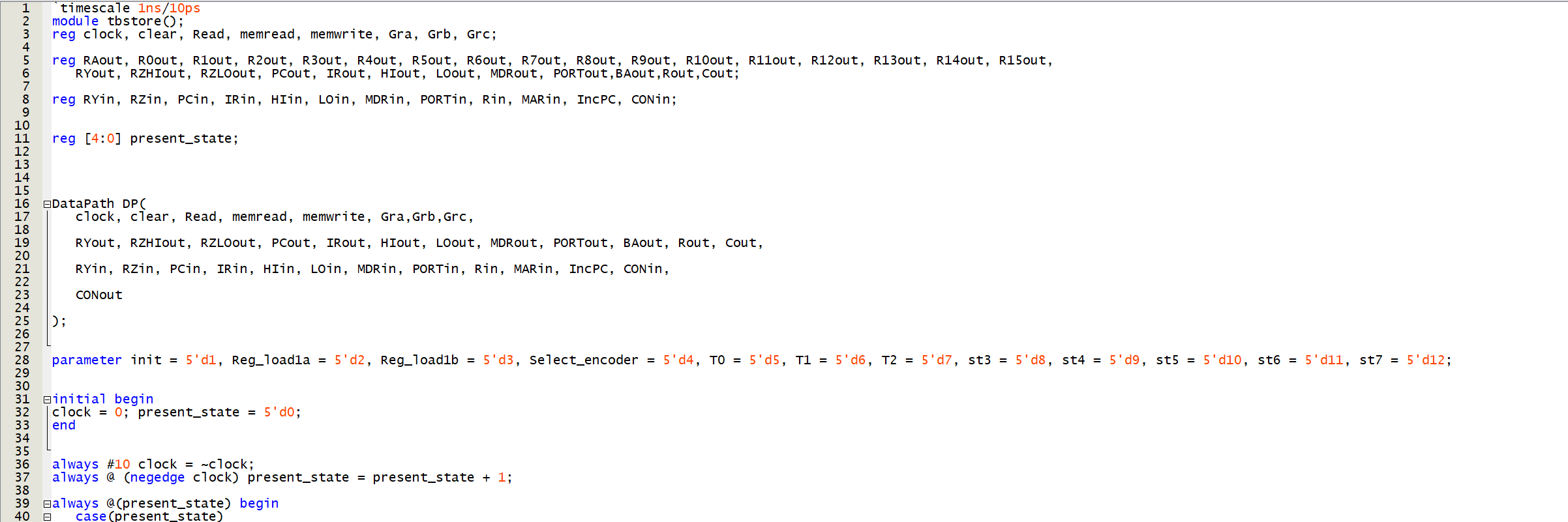
## In/Output Ports



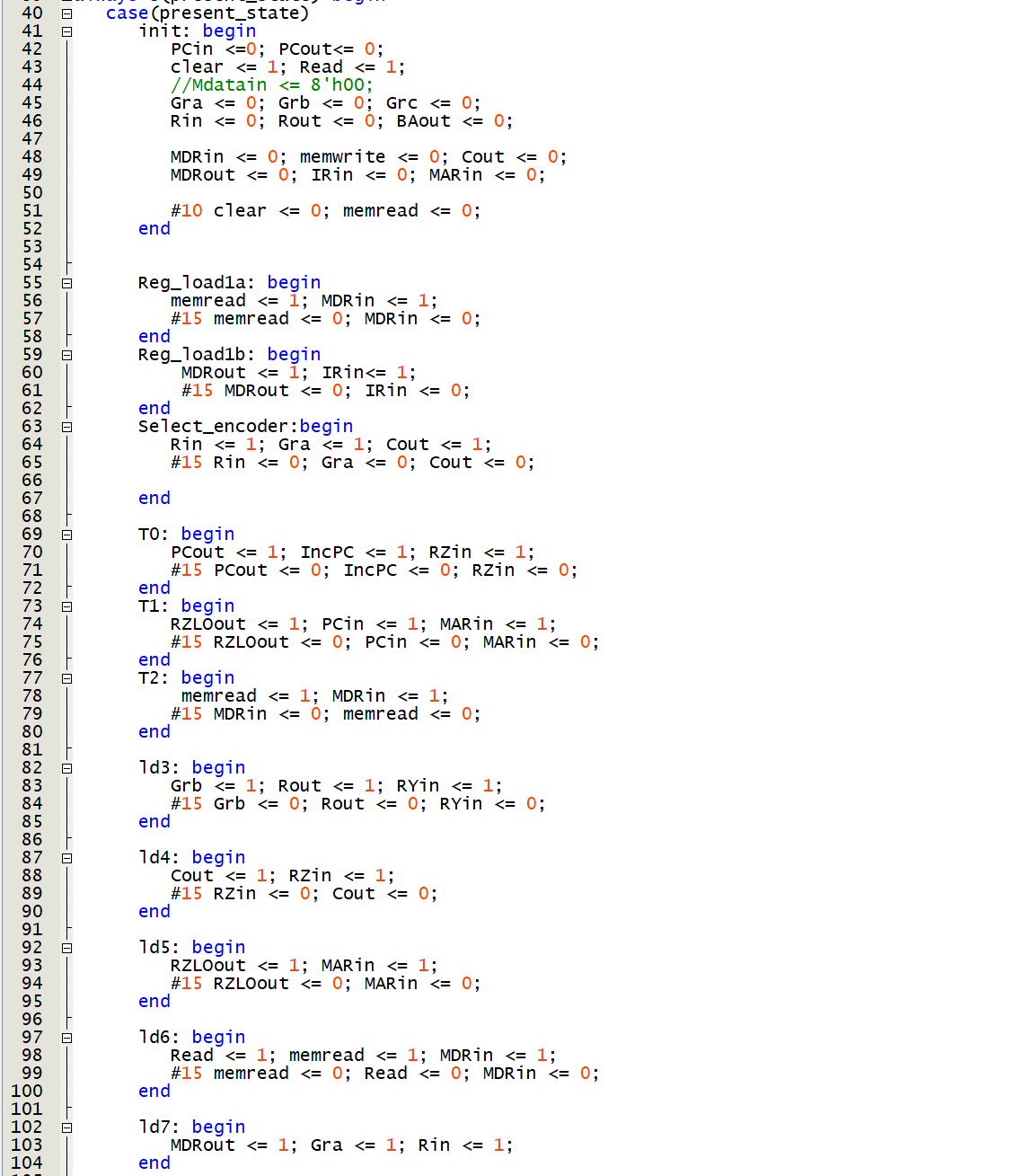


# Testbenches

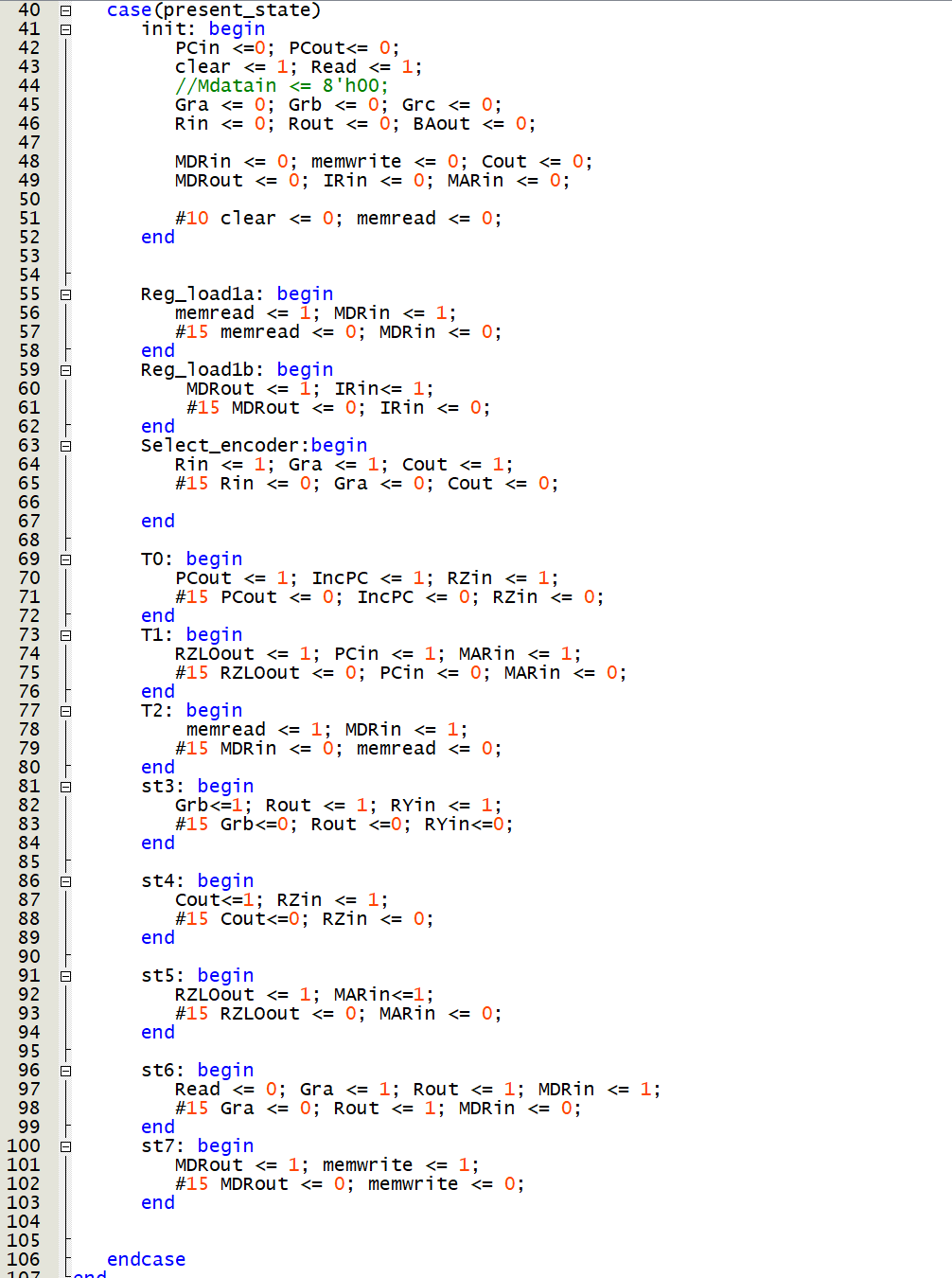
All test benches started with the following



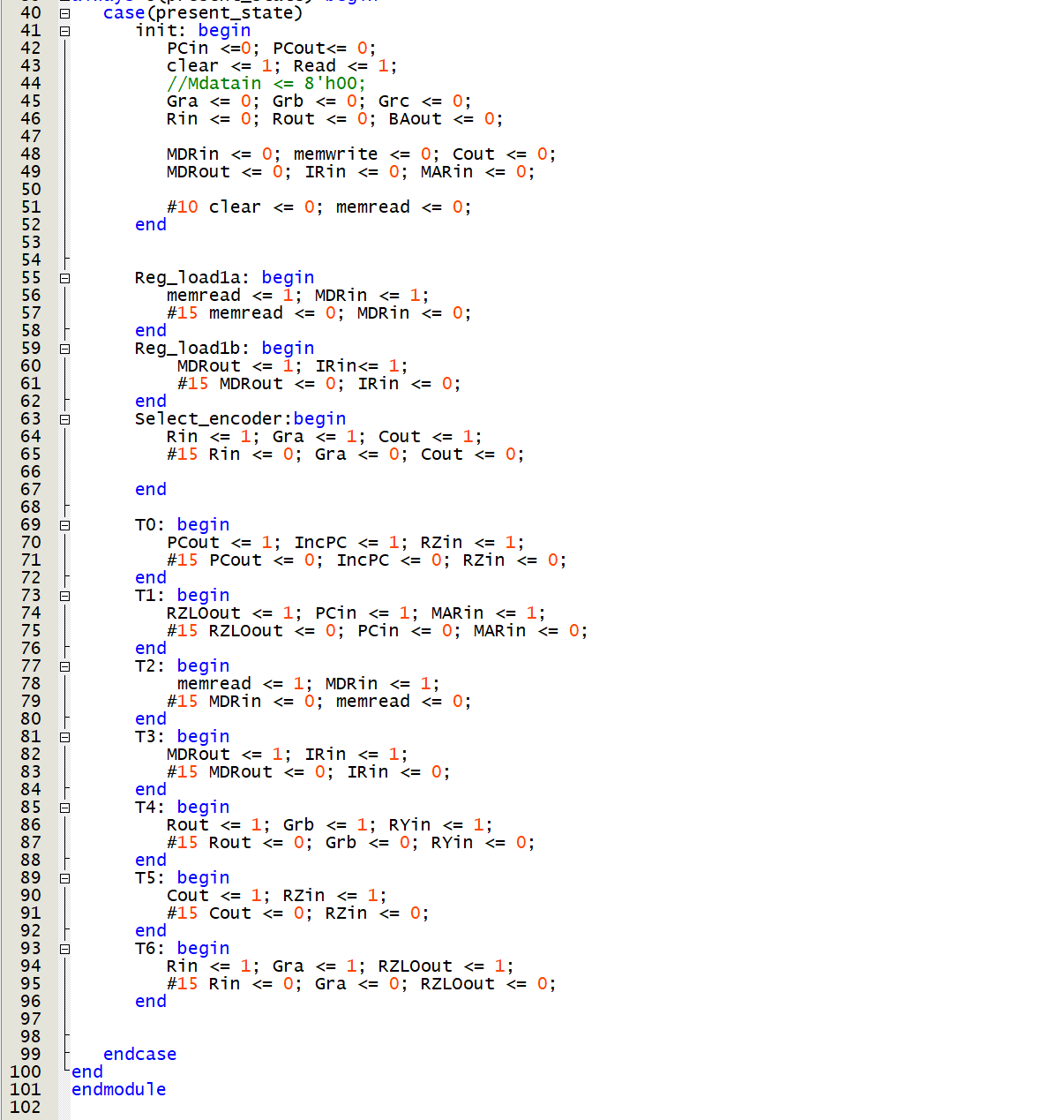
## Load



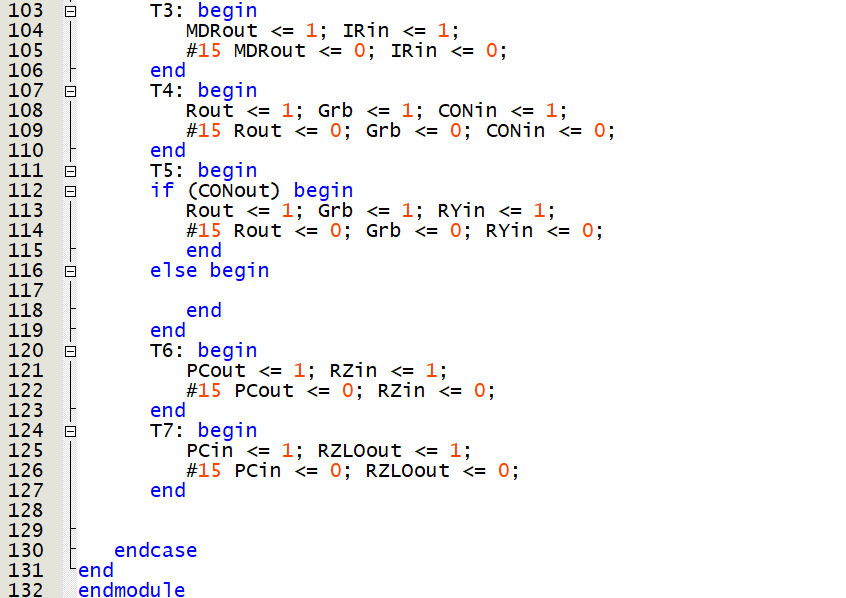
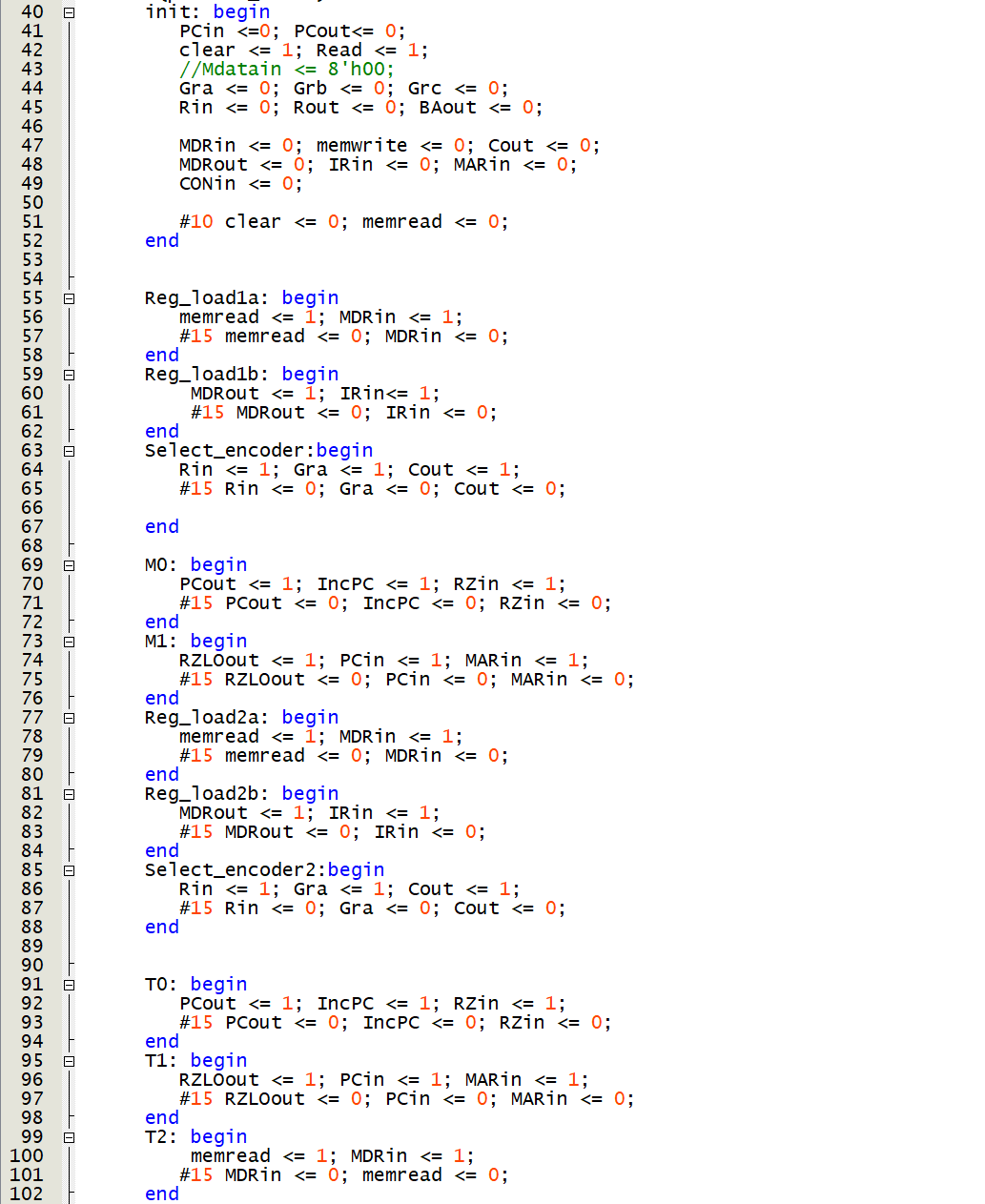
## Store



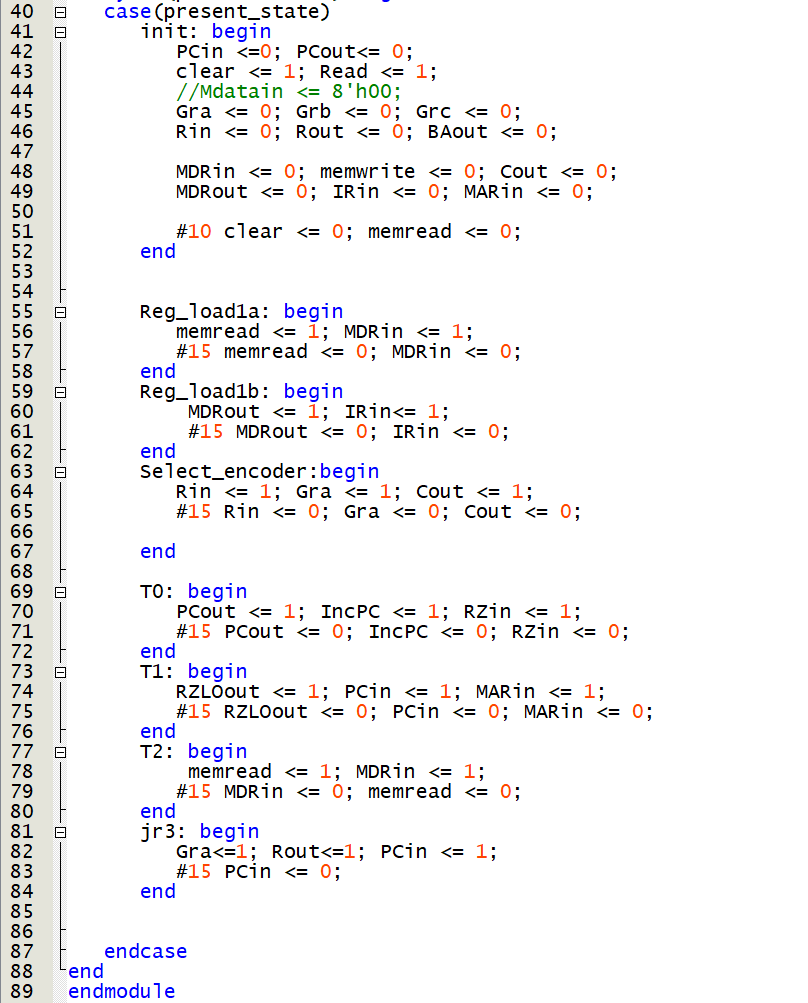
## ALU Immediate



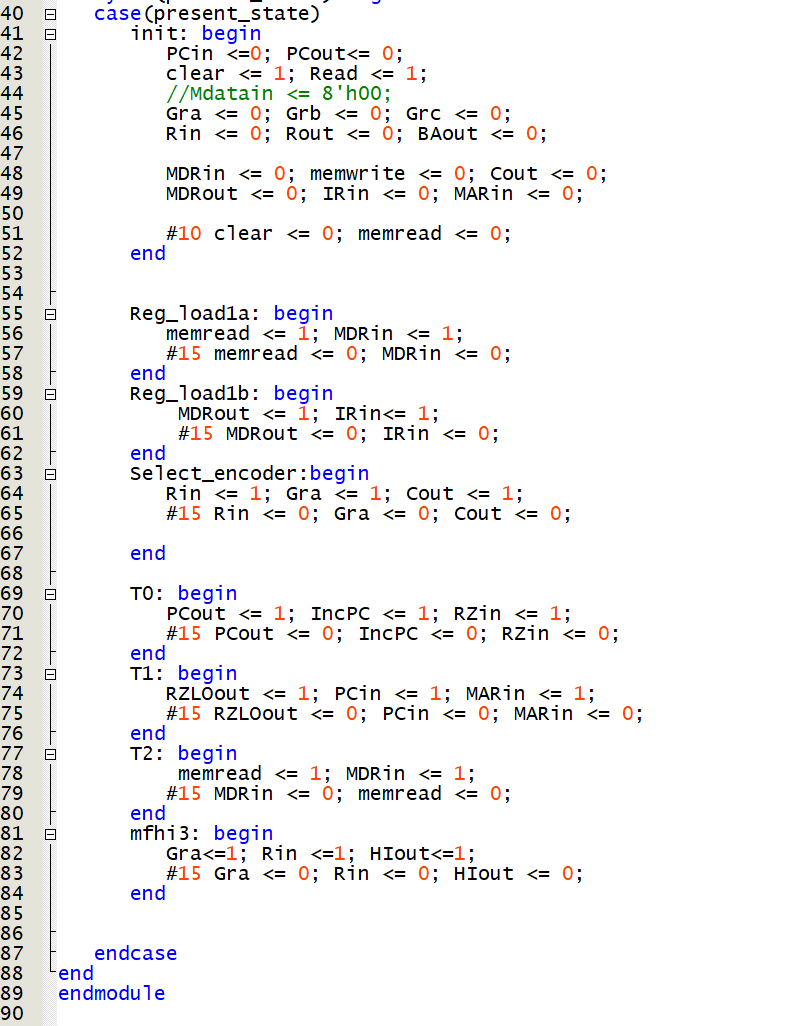
## Branch



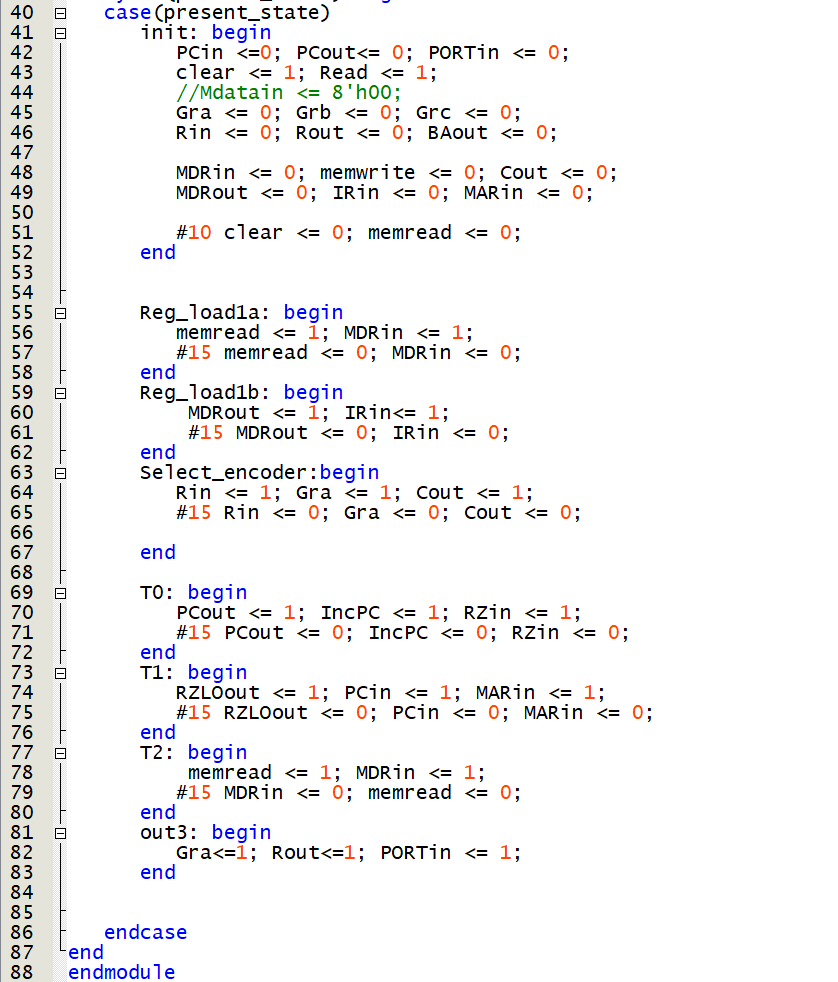
## Jump



## Mfhi/mflo



## In/outport



# Memory Printouts

Different memory was ...

## Load

## Store



## ALU Immediate



## Branch



## Jump



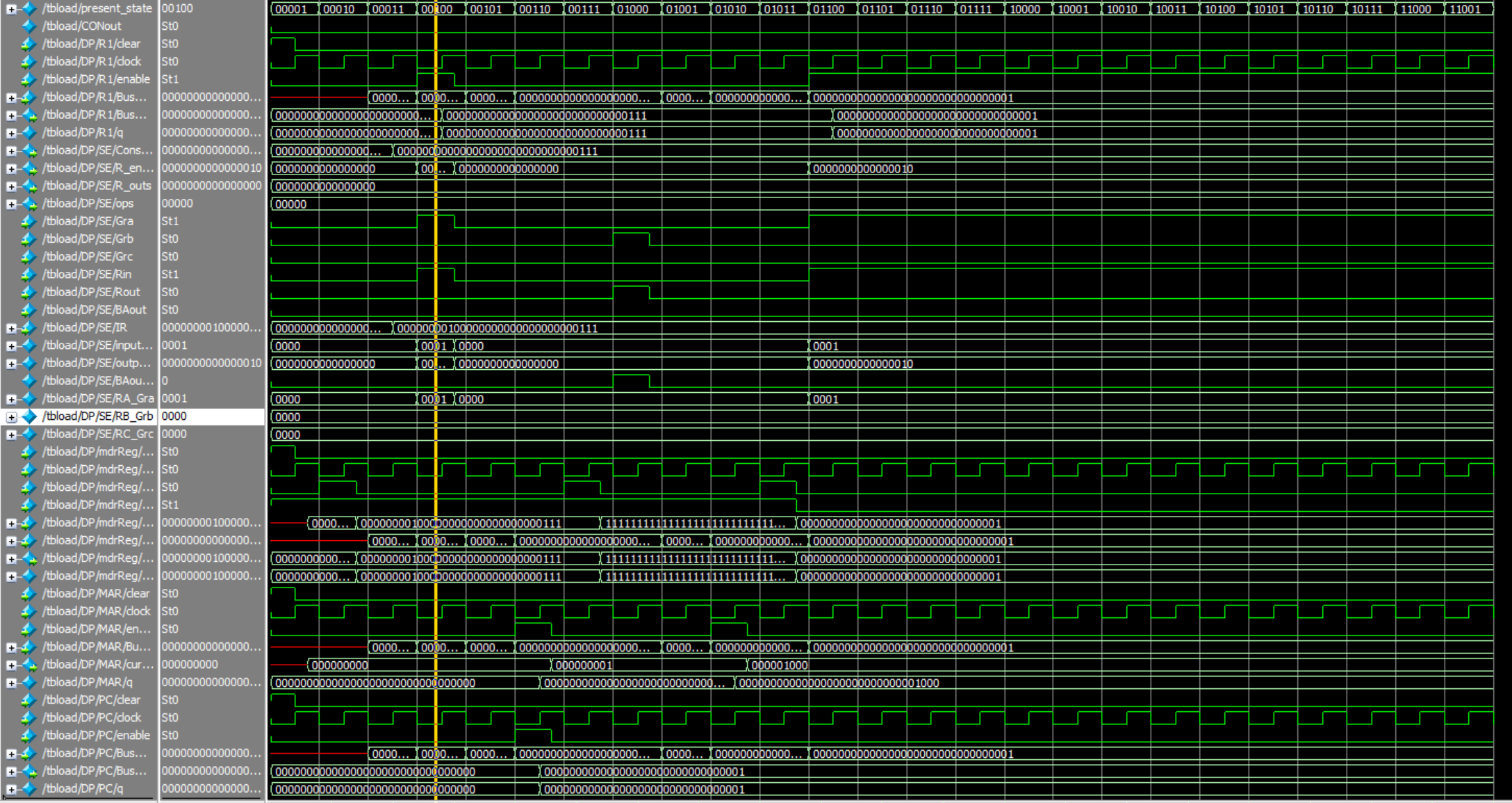
## Mfhi/mflo



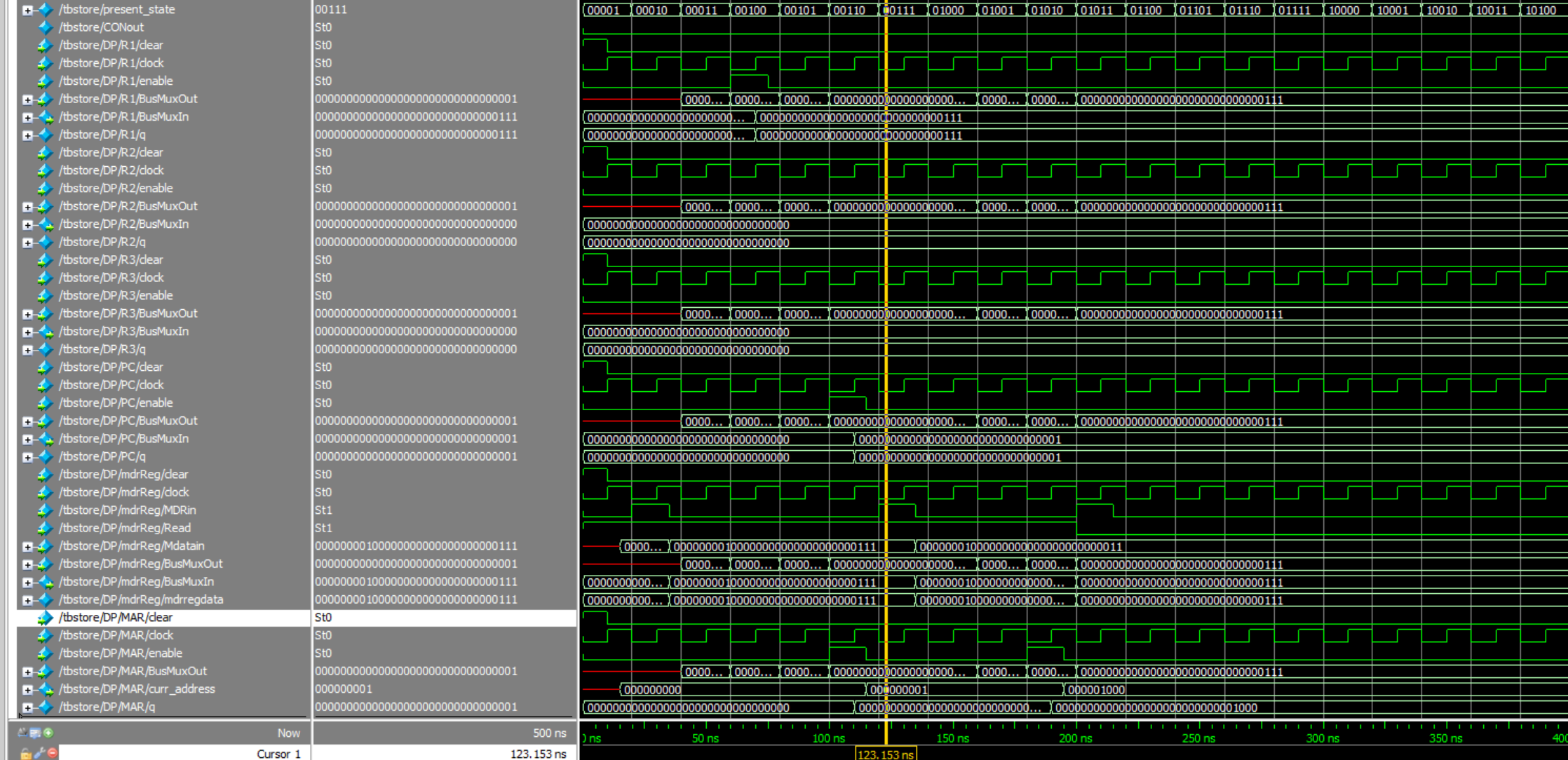
## In/outport

# Simulation Runs

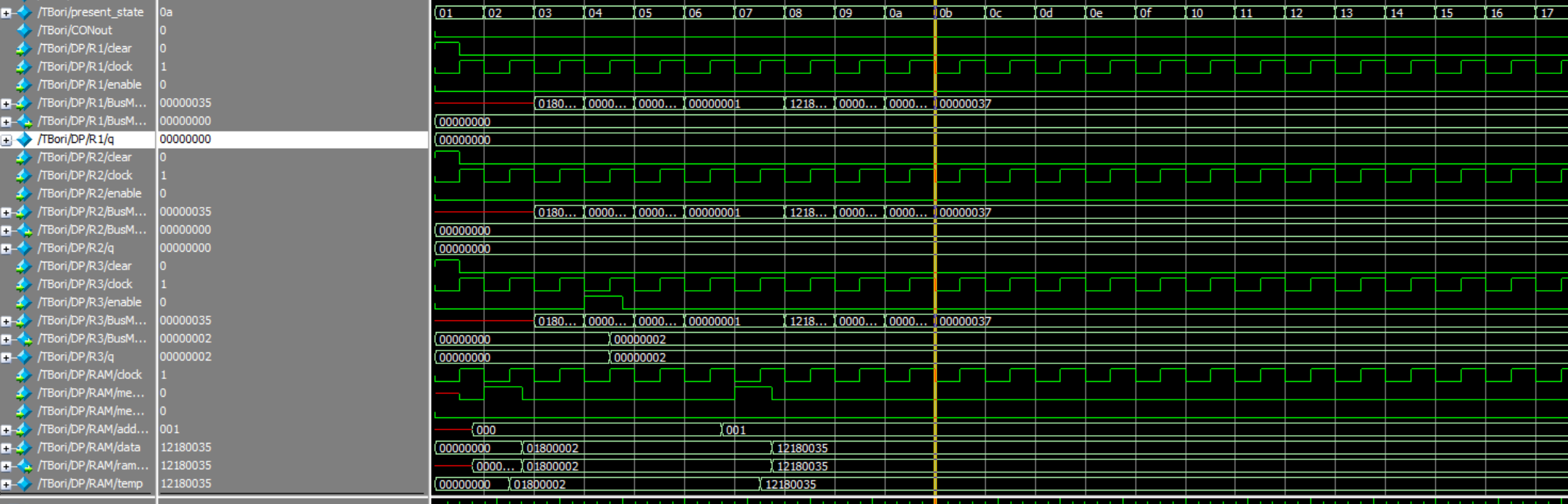
## Load



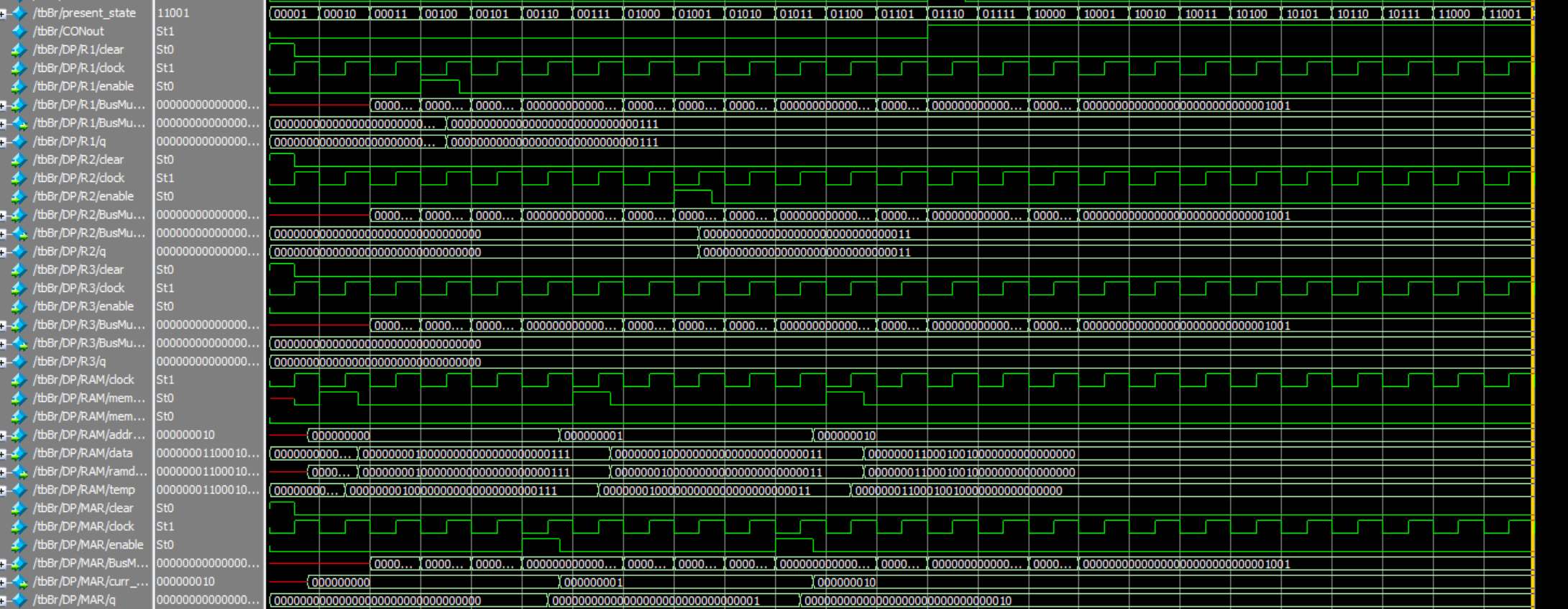
## Store



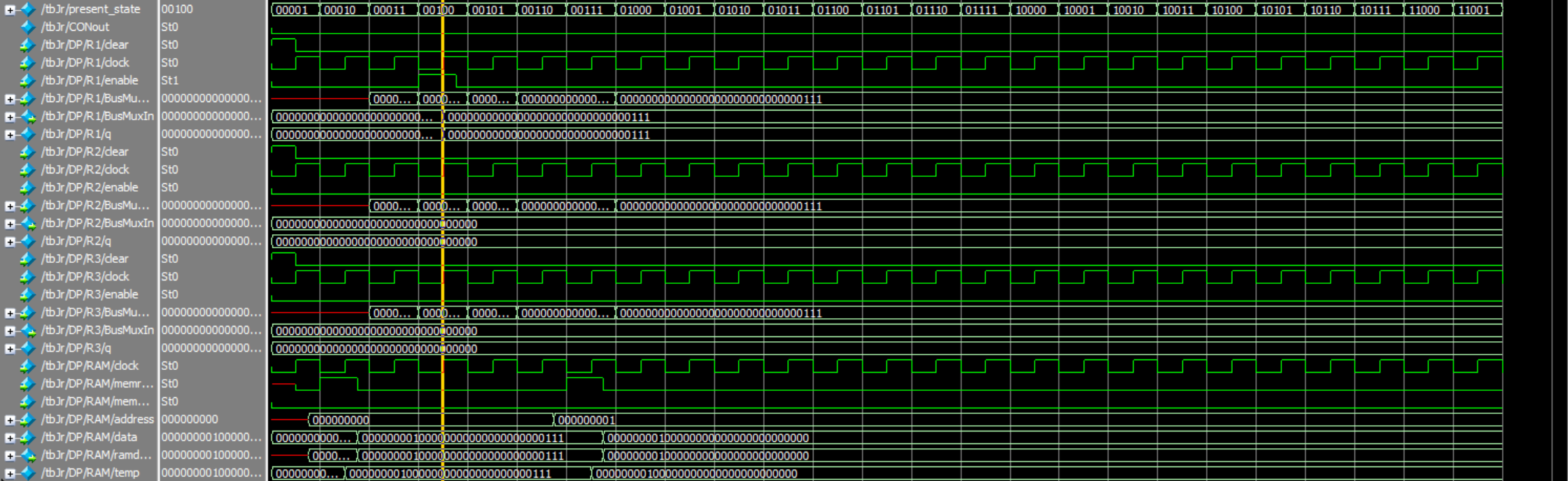
## ALU Immediate



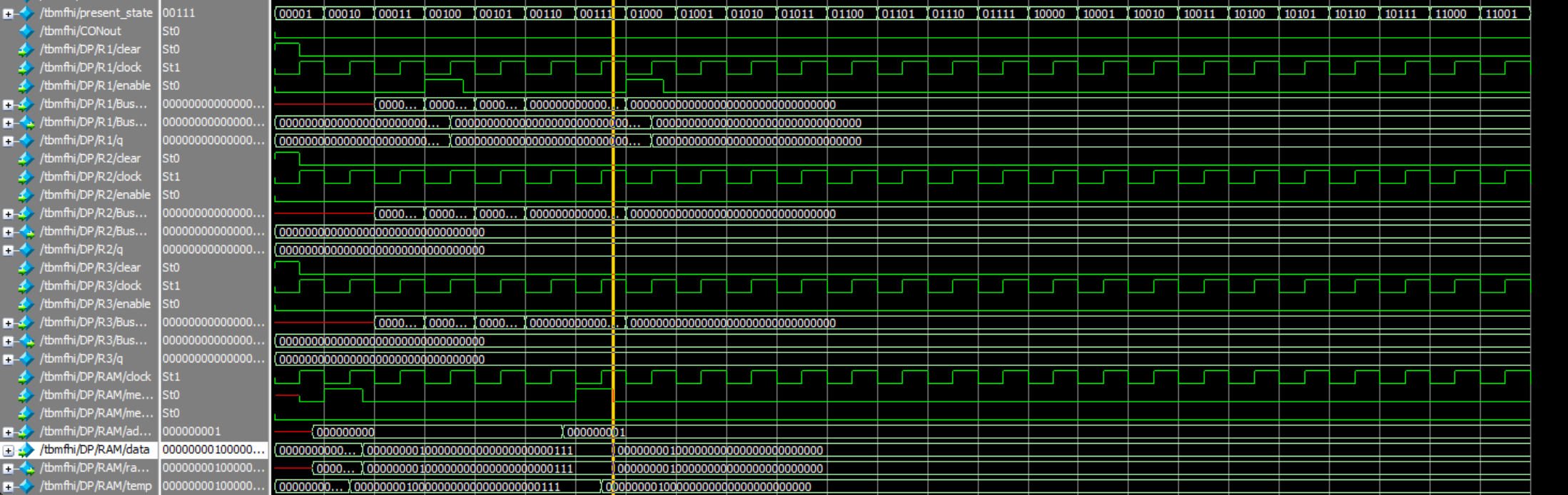
## Branch



## Jump



## Mfhi/mflo



## In/outport